

**AU9216**  
**USB Hub Controller**  
**Technical Reference Manual**

Revision 1.01

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# Table of Contents

<b>1.0 Introduction</b> .....	<b>1</b>
1.1. Description .....	1
1.2. Features .....	1
<b>2.0 Application Block Diagram</b> .....	<b>3</b>
<b>3.0 Pin Assignment</b> .....	<b>5</b>
<b>4.0 System Architecture and Reference Design</b> .....	<b>17</b>
4.1. AU9216 Block Diagram .....	17
4.2. Sample Schematics .....	18
<b>5.0 Electrical Characteristics</b> .....	<b>21</b>
5.1. Maximum Ratings .....	21
5.2. Recommended Operating Conditions .....	21
5.3. Crystal Oscillator Circuit Setup for Characterization .....	22
5.4. USB Transceiver Characteristics .....	22
5.5. ESD Test Results .....	27
5.6. Latch-Up Test Results .....	28
<b>6.0 Mechanical Information</b> .....	<b>31</b>



# 1.0 Introduction

## 1.1. Description

The AU9216 is an integrated single chip USB hub controller. It is designed to support the emerging industry Universal Serial Bus (USB) standard. The AU9216 can support up to six USB downstream ports. Each downstream port supports separated enable LED, power control and over-current sensing. Single chip integration makes the AU9216 the most cost effective stand-alone USB hub solution available in the market. USB vendor ID and Device ID can be customized via external EEPROM. Downstream ports can be used to connect various USB peripheral devices, such as USB printers, modems, scanners, cameras, mice, or joysticks, to the system without adding external glue logic.

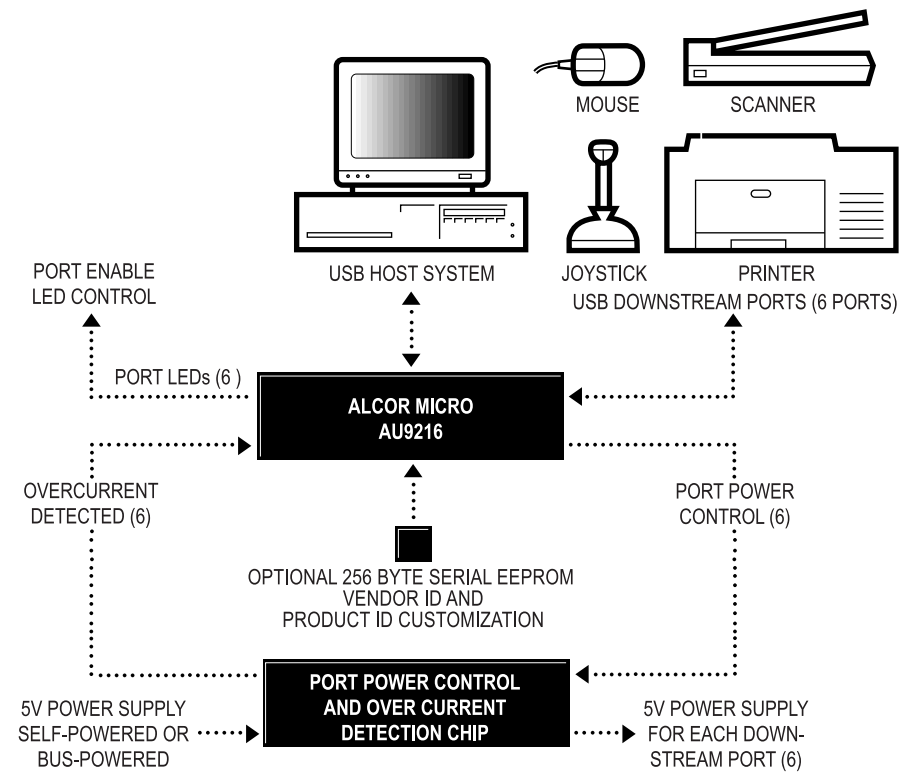
## 1.2. Features

- Fully compliant with the Universal Serial Bus Specification, version 1.0
- USB hub design is compliant with Universal Serial Bus Hub Specification, revision 1.1
- Single chip integrated USB hub controller with embedded proprietary processor
- Supports six bus-powered or self-powered downstream ports
- Supports individual port power control, LED and over-current detection
- USB vendor and device ID can be customized via external EEPROM
- Built-in default vendor ID provides cost saving if customization is not required
- Built-in 3.3v voltage regulator allows single +5V operating voltage drawing directly from USB bus. This results in reduced overall system cost.
- Runs at 12Mhz frequency
- Available in 48-pin DIP and 52-pin QFP

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## 2.0 Application Block Diagram

The AU9216 is a single chip 6-port USB hub controller. The upstream port is connected to the USB system. The downstream ports can be used for a mouse, joystick, scanner, printer or other device.



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## 3.0 Pin Assignment

The AU9216 is packaged both as a 52-pin quad flat pack (QFP) and as a 48-pin dual inline package (DIP). The following figures show the signal names for each of the pins on the chip. The tables on the following pages describe each of the pin signals

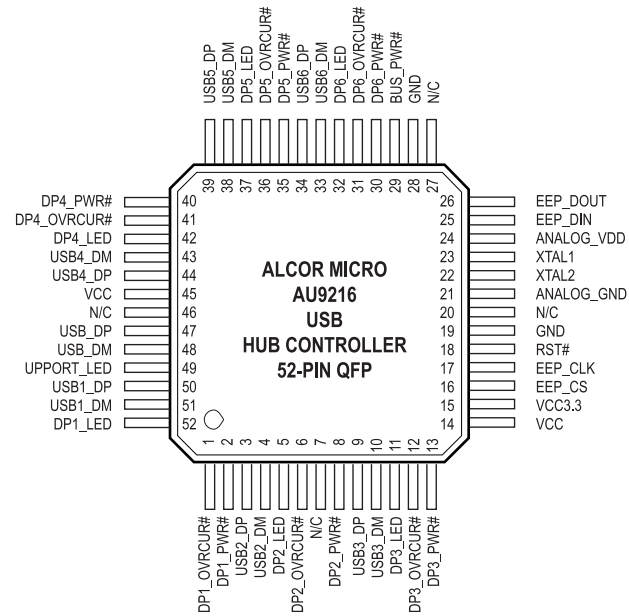


Table 3-1. Pin Descriptions for the 52-pin QFP

Pin #	Pin Name	I/O	Description
1	DP1_OVRCUR#	I	Downstream port 1 over-current indicator. Active low.
2	DP1_PWR#	O	Downstream port 1 power on. Active low.
3	USB2_DP	I/O	USB D+ for downstream port 2, add 15KΩ pull-down to ground.
4	USB2_DM	I/O	USB D- for downstream port 2, add 15KΩ pull-down to ground.

Table 3-2 (continued). Pin Descriptions for the 52-pin QFP

Pin #	Pin Name	I/O	Description
5	DP2_LED	O	Downstream port 2 LED. Active low when port 2 enabled.
6	DP2_OVRCUR#	I	Downstream port 2 over-current indicator. Active low.
7	N/C	-	No connection.
8	DP2_PWR#	O	Downstream port 2 power on. Active low.
9	USB3_DP	I/O	USB D+ for downstream port 3, add 15K $\Omega$ pull-down to ground.
10	USB3_DM	I/O	USB D- for downstream port 3, add 15K $\Omega$ pull-down to ground.
11	DP3_LED	O	Downstream port 3 LED. Active low when port 3 enabled.
12	DP3_OVRCUR#	I	Downstream port 3 over-current indicator. Active low.
13	DP3_PWR#	O	Downstream port 3 power on. Active low.
14	VCC	PWR	+5V power supply.
15	VCC3.3	O	+3.3V power. Add 1.5K pull-up on USB_DP.
16	EEP_CS	O	EEPROM chip select.
17	EEP_CLK	O	Clock for EEPROM.

Table 3-2 (continued). Pin Descriptions for the 52-pin QFP

Pin #	Pin Name	I/O	Description
18	RST#	I	Reset. Active low.
19	GND	PWR	Ground.
20	N/C	-	No connection.
21	ANALOG_GND	PWR	Analog ground.
22	XTAL2	O	Crystal, XTAL-out.
23	XTAL1	I	Crystal, XTAL-in.
24	ANALOG_VDD	PWR	Analog power, connect to +5V.
25	EEP_DIN	O	connect to EEPROM D <sub>in</sub> pin.
26	EEP_DOUT	I	Connect to EEPROM D <sub>out</sub> pin.
27	N/C	-	No connection.
28	GND	PWR	Ground.
29	BUS_PWR#	I	Bus power. One indicates bus-powered.
30	DP6_PWR#	O	Downstream port 6 power on. Active low.
31	DP6_OVRCUR#	I	Downstream port 6 over-current indicator. Active low.
32	DP6_LED	O	Downstream port 6 LED. Active low when port 6 enabled.

Table 3-2 (continued). Pin Descriptions for the 52-pin QFP

Pin #	Pin Name	I/O	Description
33	USB6_DM	I/O	USB D- for downstream port 6, add 15K $\Omega$ pull-down to ground.
34	USB6_DP	I/O	USB D+ for downstream port 6, add 15K $\Omega$ pull-down to ground.
35	DP5_PWR#	O	Downstream port 5 power on. Active low.
36	DP5_OVRCUR#	I	Downstream port 5 over-current indicator. Active low.
37	DP5_LED	O	Downstream port 5 LED. Active low when port 5 enabled.
38	USB5_DM	I/O	USB D- for downstream port 5, add 15K $\Omega$ pull-down to ground.
39	USB5_DP	I/O	USB D+ for downstream port 5, add 15K $\Omega$ pull-down to ground.
40	DP4_PWR#	O	Downstream port 4 power on. Active low.
41	DP4_OVRCUR#	I	Downstream port 4 over-current indicator. Active low.
42	DP4_LED	O	Downstream port 4 LED. Active low when port 4 enabled.
43	USB4_DM	I/O	USB D- for downstream port 4, add 15K $\Omega$ pull-down to ground.
44	USB4_DP	I/O	USB D+ for downstream port 4, add 15K $\Omega$ pull-down to ground.

Table 3-2 (continued). Pin Descriptions for the 52-pin QFP

Pin #	Pin Name	I/O	Description
45	VCC	PWR	+5V power supply.
46	N/C	-	No connection.
47	USB_DP	I/O	USB D+ for upstream port. Need external 1.5K $\Omega$ pull-up to 3.3V.
48	USB_DM	I/O	USB D- for upstream port.
49	UPPORT_LED	O	Upstream port LED. Active low when upstream port enabled.
50	USB1_DP	I/O	USB D+ for downstream port 1, add 15K $\Omega$ pull-down to ground.
51	USB1_DM	I/O	USB D- for downstream port 1, add 15K $\Omega$ pull-down to ground.
52	DP1_LED	O	Downstream port 1 LED. Active low when port 1 enabled.

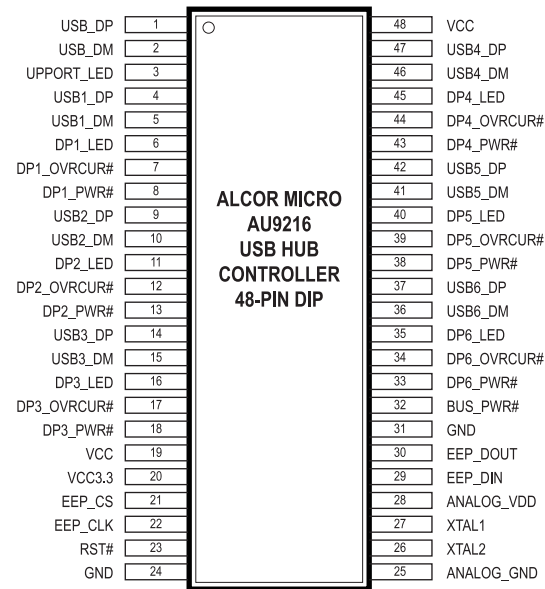


Table 3-2. Pin Descriptions for the 48-pin DIP

Pin #	Pin Name	I/O	Description
1	USB_DP	I/O	USB D+ for upstream port. Need external 1.5K $\Omega$ pull-up to 3.3V.
2	USB_DM	I/O	USB D- for upstream port.
3	UPPORT_LED	O	Upstream port LED. Active low when upstream port enabled.
4	USB1_DP	I/O	USB D+ for downstream port 1, add 15K $\Omega$ pull-down to ground.

Table 3-2 (continued). Pin Descriptions for the 48-pin DIP

Pin #	Pin Name	I/O	Description
5	USB1_DM	I/O	USB D- for downstream port 1, add 15K $\Omega$ pull-down to ground.
6	DP1_LED	O	Downstream port 1 LED. Active low when port1 enabled.
7	DP1_OVRCUR#	I	Downstream port 1 over-current indicator. Active low.
8	DP1_PWR#	O	Downstream port 1 power on. Active low.
9	USB2_DP	I/O	USB D+ for downstream port 2, add 15K $\Omega$ pull-down to ground.
10	USB2_DM	I/O	USB D- for downstream port 2, add 15K $\Omega$ pull-down to ground.
11	DP2_LED	O	Downstream port 2 LED. Active low when port 2 enabled.
12	DP2_OVRCUR#	I	Downstream port 2 over-current indicator. Active low.
13	DP2_PWR#	O	Downstream port 2 power on. Active low.
14	USB3_DP	I/O	USB D+ for downstream port 3, add 15K $\Omega$ pull-down to ground.
15	USB3_DM	I/O	USB D- for downstream port 3, add 15K $\Omega$ pull-down to ground.
16	DP3_LED	O	Downstream port 3 LED. Active low when port 3 enabled.
17	DP3_OVRCUR#	I	Downstream port 3 over-current indicator. Active low.
18	DP3_PWR#	O	Downstream port 3 power on. Active low.

Table 3-2 (continued). Pin Descriptions for the 48-pin DIP

Pin #	Pin Name	I/O	Description
19	VCC	PWR	+5V power supply.
20	VCC3.3	O	+3.3V power. Add 1.5K pull-up on USB_DP.
21	EEP_CS	O	EEPROM chip select.
22	EEP_CLK	O	Clock for EEPROM.
23	RST#	I	Reset. Active low.
24	GND	PWR	Ground.
25	ANALOG_GND	PWR	Analog ground.
26	XTAL2	O	Crystal, XTAL-out.
27	XTAL1	I	Crystal, XTAL-in.
28	ANALOG_VDD	PWR	Analog power, connect to +5V.
29	EEP_DIN	O	connect to EEPROM D <sub>in</sub> pin.
30	EEP_DOUT	I	Connect to EEPROM D <sub>out</sub> pin.
31	GND	PWR	Ground.
32	BUS_PWR#	I	Bus power. One indicates bus-powered.
33	DP6_PWR#	O	Downstream port 6 power on. Active low.
34	DP6_OVRCUR#	I	Downstream port 6 over-current indicator. Active low.

Table 3-2 (continued). Pin Descriptions for the 48-pin DIP

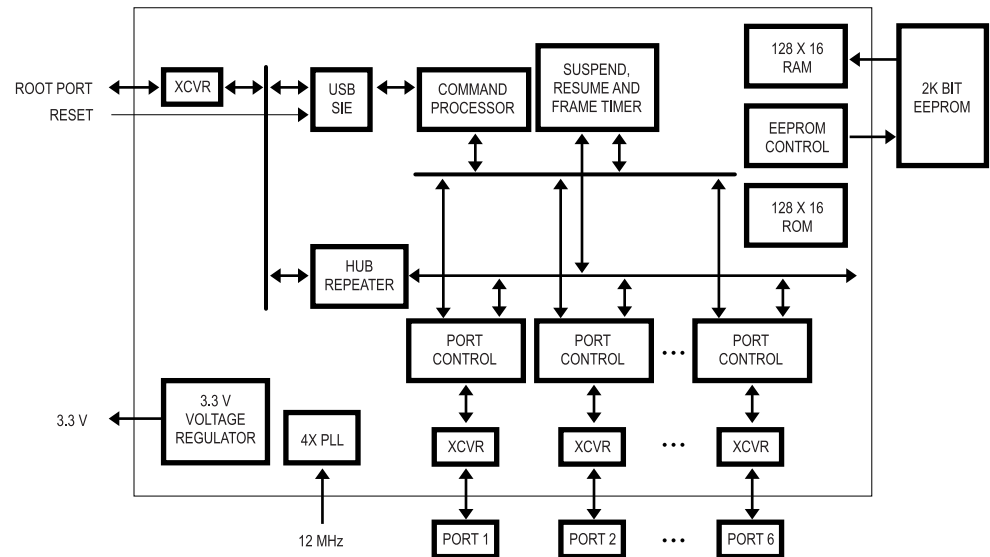
Pin #	Pin Name	I/O	Description
35	DP6_LED	O	Downstream port 6 LED. Active low when port 6 enabled.
36	USB6_DM	I/O	USB D- for downstream port 6, add 15K $\Omega$ pull-down to ground.
37	USB6_DP	I/O	USB D+ for downstream port 6, add 15K $\Omega$ pull-down to ground.
38	DP5_PWR#	O	Downstream port 5 power on. Active low.
39	DP5_OVRCUR#	I	Downstream port 5 over-current indicator. Active low.
40	DP5_LED	O	Downstream port 5 LED. Active low when port 5 enabled.
41	USB5_DM	I/O	USB D- for downstream port 5, add 15K $\Omega$ pull-down to ground.
42	USB5_DP	I/O	USB D+ for downstream port 5, add 15K $\Omega$ pull-down to ground.
43	DP4_PWR#	O	Downstream port 4 power on. Active low.
44	DP4_OVRCUR#	I	Downstream port 4 over-current indicator. Active low.
45	DP4_LED	O	Downstream port 4 LED. Active low when port 4 enabled.
46	USB4_DM	I/O	USB D- for downstream port 4, add 15K $\Omega$ pull-down to ground.
47	USB4_DP	I/O	USB D+ for downstream port 4, add 15K $\Omega$ pull-down to ground.

Table 3-2 (continued). Pin Descriptions for the 48-pin DIP

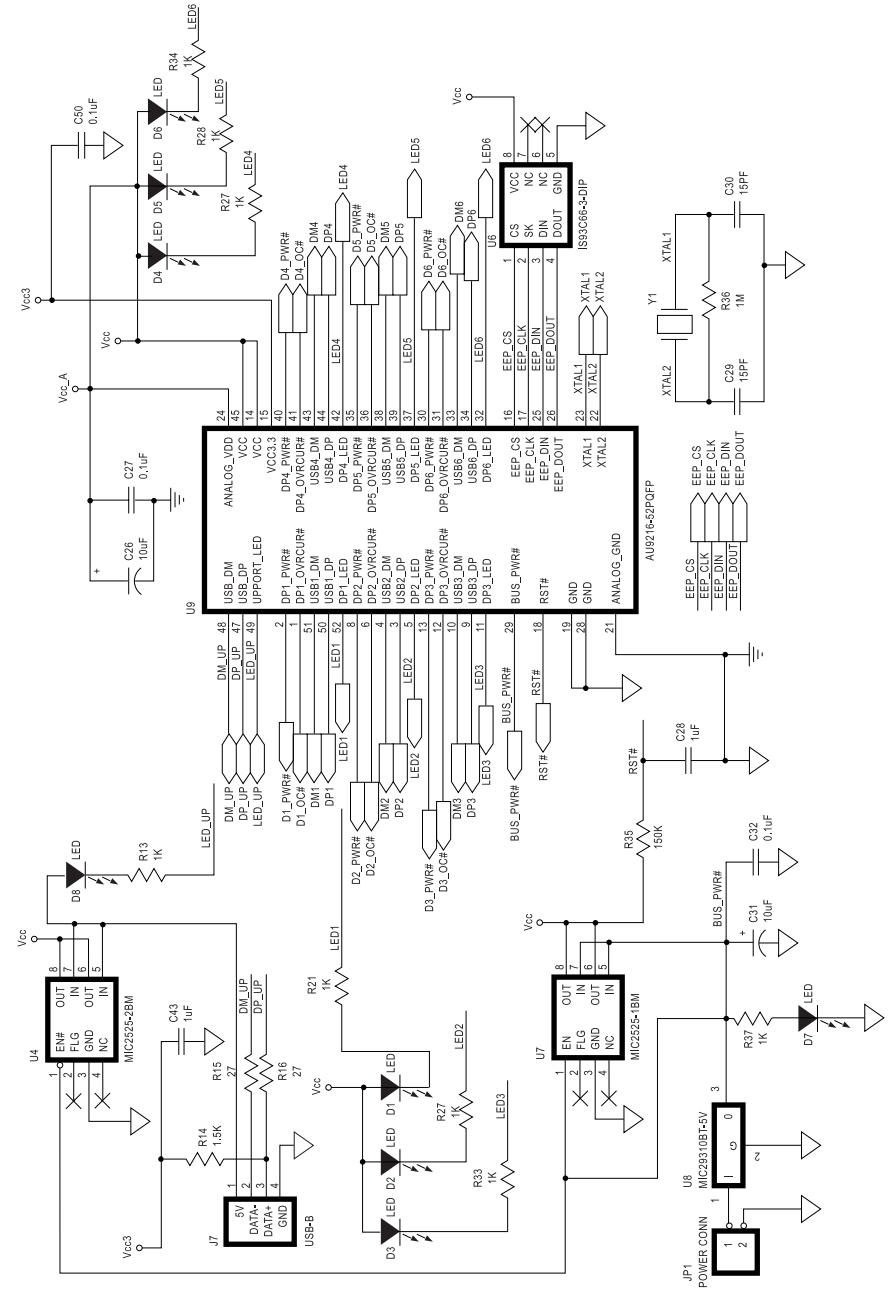
Pin #	Pin Name	I/O	Description
48	VCC	PWR	+5V power supply.

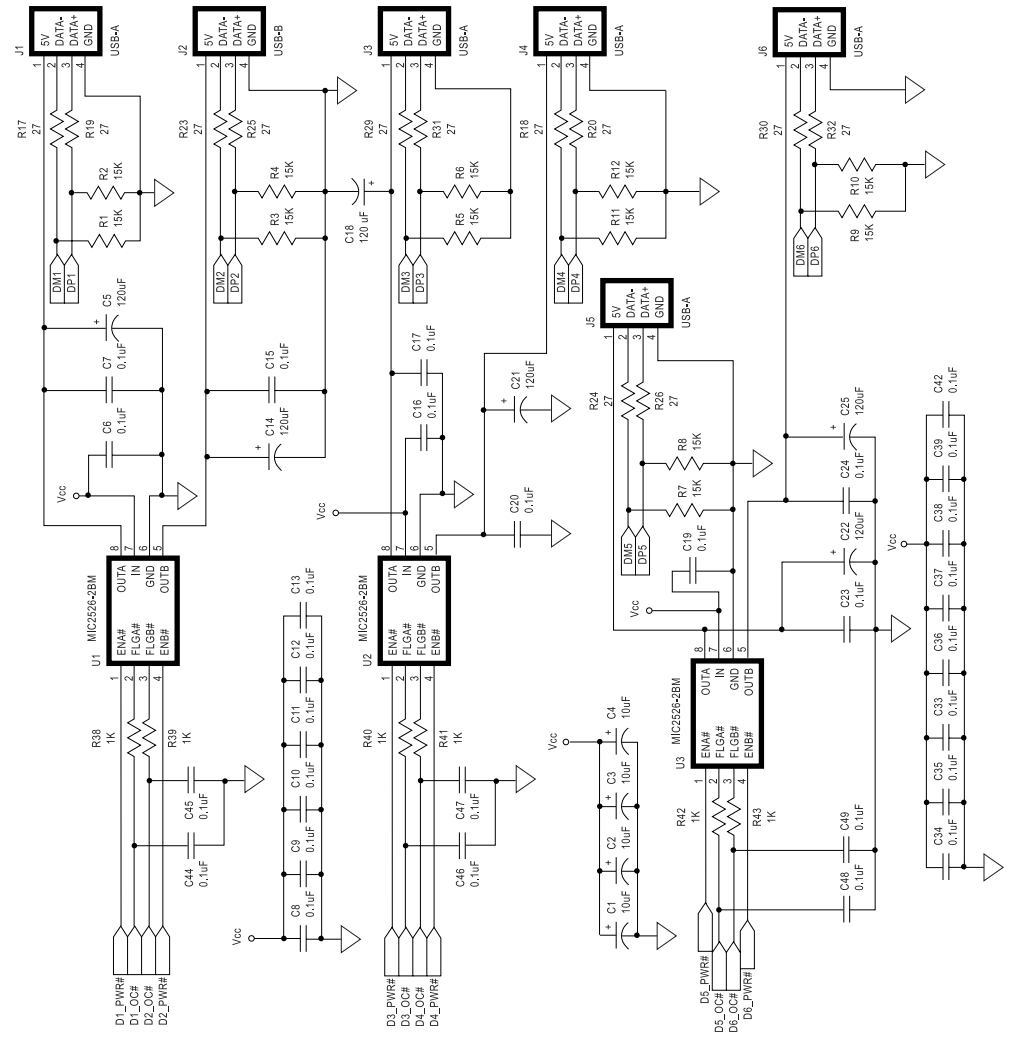
# 4.0 System Architecture and Reference Design

## 4.1. AU9216 Block Diagram



## 4.2. Sample Schematics





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# 5.0 Electrical Characteristics

## 5.1. Maximum Ratings

### Absolute Maximum Ratings

PARAMETER	VALUES	
	MIN	MAX
Ambient Operating Temperatures	0°C	70°C
Storage Temperature	-40°C	185°C
Supply Voltage (Vdd)	-0.3V	7.0V

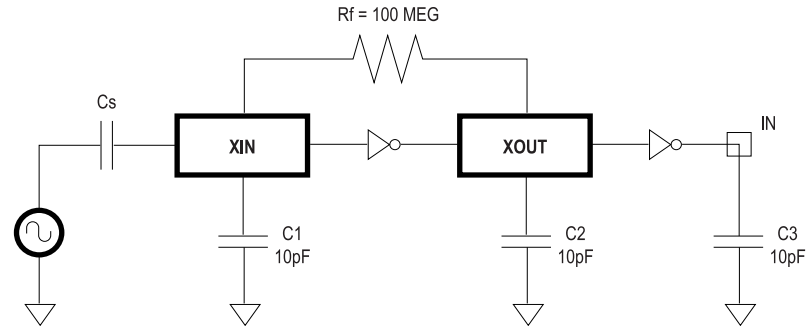
## 5.2. Recommended Operating Conditions

The following table gives the recommended operating conditions for integrated circuits developed with the pad libraries:

Symbol	Param.	Min	Max	V <sub>DD</sub>	Note
V <sub>IL</sub>	Low level input voltage	-0.5V	0.8V	4.5V to 5.5V	Guaranteed Input Low Voltage
V <sub>IH</sub>	High level input voltage	2.0V	V <sub>DD</sub> +0.5V	4.5V to 5.5V	Guaranteed Input High Voltage
V <sub>OL</sub>	Low level output voltage		0.4V	4.5V	I <sub>OL</sub> , 2 to 24 mA(TTL), depending on Cell
V <sub>OH</sub>	High level output voltage	2.4V		4.5V	I <sub>OH</sub> , 2 to 24mA(TTL) depending on Cell
I <sub>CC</sub>	Supply current	20 mA	25 mA	4.5V to 5.5V	

### 5.3. Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor,  $C_s$ , is much larger than  $C_1$  and  $C_2$ .



### 5.4. USB Transceiver Characteristics

#### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{cc}$	DC supply voltage		3.0	3.5	V
$V_i$	DC input voltage range		0	5.5	V
$V_{iO}$	DC input range for I/Os		0	$V_{cc}$	V
$V_o$	DC output voltage range		0	$V_{cc}$	V
$T_{AMB}$	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	0	70	°C

### ABSOLUTE MAXIMUM RATINGS 1,2

In accordance with the Absolute Maximum Rating System, Voltages are referenced to GND (Ground=0v)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage		-0.5	+6.5	V
$V_{IK}$	DC input diode current	$V_i < 0$		-50	mA
$V_i$	DC input voltage	Note 3	-0.5	+5.5	V
$V_{VO}$	DC input voltage range for I/Os		-0.5	$V_{CC} + 0.5$	V
$V_{OK}$	DC output diode current	$V_o > V_{CC}$ or $V_o < 0$		+/-50	mA
$V_o$	DC output voltage	Note 3	-0.5	$V_{CC} + 0.5$	V
$V_o$	DC output source sink current for VP/VM and RCV pins	$V_o = 0$ to $V_{CC}$		+/-15	mA
$V_o$	DC output source or sink current for D+/D- pins	$V_o = 0$ to $V_{CC}$		+/-50	mA
$I_{GND}^*, I_{GND}$	DC Vcc or GND current			+/-100	mA
$T_{STG}$	Storage temperature range		-60	+/-150	°C
$P_{TOT}$	Power dissipation per package				mW

#### NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The performance capability of a high performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (Ground=0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS -40°C to +86°C			UNIT
			MIN	TYP	MAX	
VHYS	Hysteresis on inputs	V <sub>cc</sub> =3.0V to 3.6V	5.2	4.3	50.4	V
VIH	HIGH level input	V <sub>cc</sub> =3.0V to 3.6V		15	20	V
VIL	LOW level input	V <sub>cc</sub> =3.0V to 3.6V	0.5	11		V
RoH	Output impedance (HIGH state)	Note 2	28	34	43	ohm
RoL	Output impedance (LOW state)	Note 2	28	35	43	ohm
VOH	HIGH level output	V <sub>cc</sub> =3.0V I <sub>o</sub> =6mA V <sub>cc</sub> =3.0V I <sub>o</sub> =4mA V <sub>cc</sub> =3.0V I <sub>o</sub> =100μA	2.2 2.4 2.8	2.7		V
VOL	LOW level output	V <sub>cc</sub> =3.0V I <sub>o</sub> =6mA V <sub>cc</sub> =3.0V I <sub>o</sub> =4mA V <sub>cc</sub> =3.0V I <sub>o</sub> =100μA		0.3	0.7 0.4 0.2	V
IQ	Quiescent supply current	V <sub>cc</sub> =3.6V V <sub>I</sub> =V <sub>cc</sub> or GND I <sub>o</sub> =0		330	600	μA
I <sub>sup</sub>	Supply current in suspend	V <sub>cc</sub> =3.6V V <sub>I</sub> =V <sub>cc</sub> or GND I <sub>o</sub> =0			70	μA
IFS	Active supply current (Full Speed)	V <sub>cc</sub> =3.3V		9	14	mA
ILS	Active supply current (Low Speed)	V <sub>cc</sub> =3.3V		2		mA
I <sub>Leak</sub>	Input leakage current	V <sub>cc</sub> =3.6V V <sub>I</sub> =5.5V or GND, not for I/O Pins		+/- 0.1	+/- 0.5	μA
IOFF	3-state output OFF-state current	V <sub>I</sub> =V <sub>IN</sub> or V <sub>II</sub> , V <sub>o</sub> =V <sub>cc</sub> or GND			+/-1-	μA

**NOTES:**

1. All typical values are at V<sub>cc</sub>=3.3V and T<sub>amb</sub>=25°C.
2. This value includes an external resistor of 24 ohm +/-1%. See "Load D+ and D-" diagram for testing details.
3. All signals except D+ and D-.

### AC ELECTRICAL CHARACTERISTICS

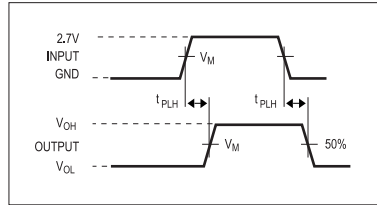
GND=0V, Is = IS=3.0 C=50pf, RL=500ohms

SYMBOL	PARAMETER	WAVFORM	LIMITS					UNIT
			-40°C to +86°C			-40°C to +86°C		
			MIN	TYP	MAX	MIN	MAX	
tpLH tpHL	VMO/VPO to D+/D- Full Speed	1	0 0		12 12	0 0	14 14	ns
trise tfall	Rise and Fall Times Full Speed	2	4 4	9 9	20 20	4 4	20 20	ns
tRFM	Rise and Fall Time Matching Full Speed		90		110	90	110	%
tpLH tpHL	VMO/VPO to D+/D- Low Speed	1		120 120	300 300		300 300	ns
trise tfall	Rise and Fall Times Low Speed	2	75 75		300 200	75 75	300 200	ns
tRFM	Rise and Fall Time Matching Low Speed		70		130	70	130	%
tpLH tpHL	D+/D- to RCV	3		9 9	16 16		16 16	ns
tpLH tpHL	D+/D- to VP/VM	1		4 4	8 8		8 8	ns
tpHZ tpZH tpLZ tpZL	OE# to D+/D- RL = 500ohm	4			12 12 10 10		12 12 10 10	ns
	Setup for SPEED	5	0					ns
Vcp	Crossover point <sup>1</sup>	3	1.3		2.0	1.3	2.0	V

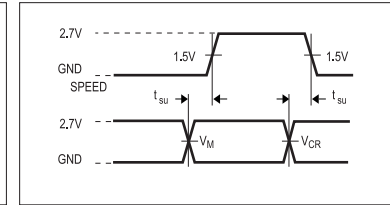
#### NOTES:

1. The crossover point is in the range of 1.3V to 2.5V for the low speed mode with a 5Cpf capacitance.

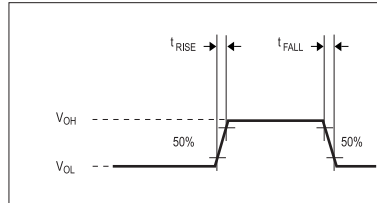
**WAVEFORM 1.**  
D+/D- TO VP/VM OR VPO/VMO TO D+/D-



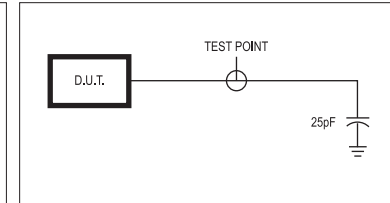
**WAVEFORM 5.**  
SETUP FOR SPEED



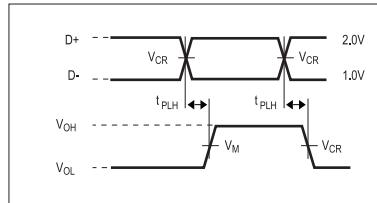
**WAVEFORM 2.**  
D+/D- TO VP/VM OR VPO/VMO TO D+/D-



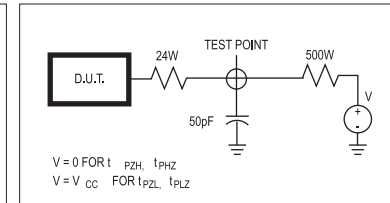
**LOAD FOR VM/VP AND RCV**



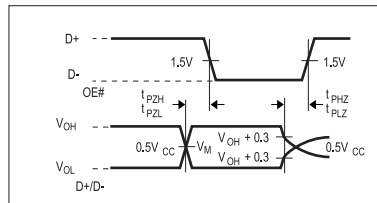
**WAVEFORM 3.**  
D+/D- TO RCV



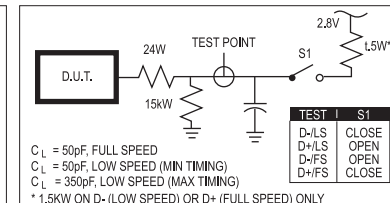
**LOAD FOR ENABLE AND DISABLE TIMES**



**WAVEFORM 4.**  
OE# TO D+/D-



**LOAD FOR D+/D-**



## 5.5. ESD Test Results

**Test Description:** ESD Testing was performed on a Zapmaster system using the Human-Body-Model (HBM) and Machine-Model (MM), according to MIL-STD 883 and EIAJ IC-121 respectively.

- Human-Body-Model stresses devices by sudden application of a high voltage supplied by a 100pF capacitor through 1.5k-ohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200pF capacitor through very low (0 ohm) resistance.

### Test Circuit & Condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

### ESD Data

Model	Mode	S/S	Target	Results
HBM	Vdd, Vss, I/C	15	2000V	PASS
MM	Vdd, Vss, I/C	15	200V	PASS

## 5.6. Latch-Up Test Results

**Test Description:** Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5Volts and ground respectively.

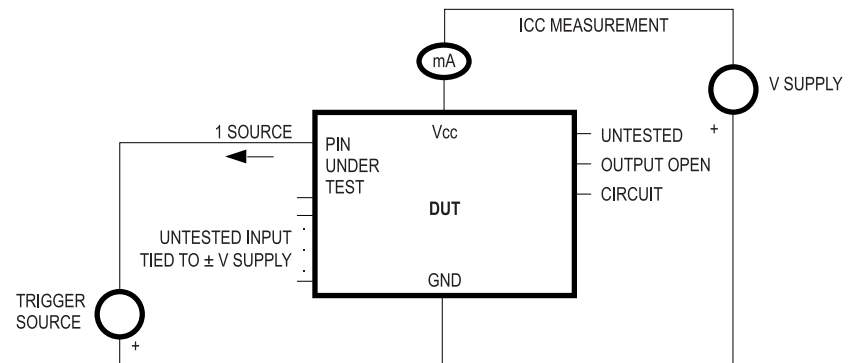
Testing was started at 5.0V (Positive) or 0V (Negative), and the DUT was biased for 0.5 seconds.

If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=00mA, Icc=100mA), then the voltage was increased by 0.1Volts and the pin was tested again.

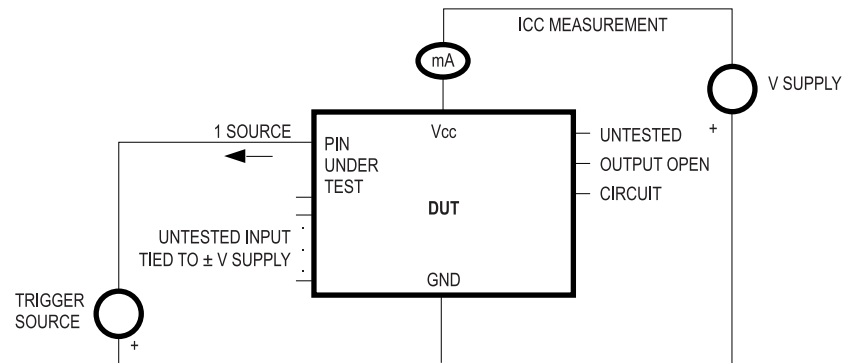
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

### Notes:

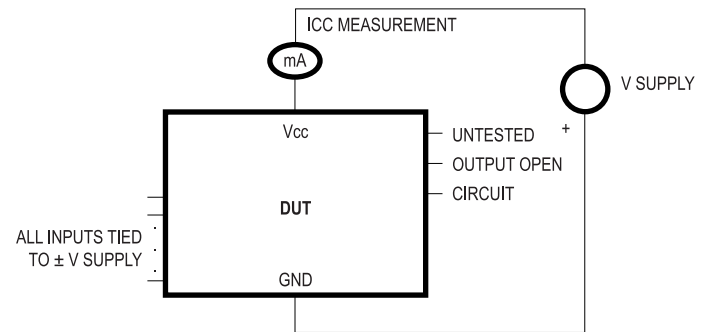
1. DUT: The device under test.
2. PUT: The pin under test.



**Test Circuit: Positive Input/Output Overvoltage/Overcurrent**



**Test Circuit: Negative Input/Output Overvoltage/Overcurrent**



**Supply Overvoltage Test**

**Latch-Up Data**

Mode		Voltage (V)/Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0	5	Pass
Current	+	200	5	Pass
	-	200	5	Pass
Vdd - Vxx		9.0	5	Pass

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## 6.0 Mechanical Information

Following diagrams show the dimensions of the AU9216 52-pin QFP and the 48-pin DIP packages. Measurements are in millimeters; measurements in parenthesis are in inches.

